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Following Paper ID and Roll No. to be filled in your Answer Book.

PAPER ID : 33227 Roll No.

B. Tech. Examination 2021-22

(Even Semester)

ADVANCED COMPUTER ARCHITECTURE

Time : Three Hours] *[Maximum Marks : 60*

Note :– Attempt all questions.

SECTION – A

1. Attempt all parts of the following : $8 \times 1 = 8$

   (a) Draw the block diagram of shared memory architecture.

   (b) What is the Bernstein conditions in context to parallelism and dependence relations?

   (c) What is pipelining?

   (d) Define cluster computers.

   (e) Define HIT ratio.

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(f) What is latency?

(g) Consider the given alorithms

```
1:  // Original code
2:  For i=1 to n do
3:  b[i] =a [i] + 1.0;
4:  end for
5:  for i = 1 to n do
6:  c [i] = b[i] *4.0;
7:  end for
```

Transform the algorithms by using loop fusion method.

(h) Write the storage capacity range of L1, L2 and L3 cache memory modules.

SECTION–B

2. Attempt any two parts of the following : $6 \times 2 = 12$

(a) Write difference between fine-grained and coarse-grained SIMD Architecture.

(b) Define the instruction level parallelism (ILP), suppose that, four operations can be carried out in single clock cycle. There will be four functional units, each attached to one of the operations, branch unit, and common register file in the ILP execution hardware. The sub-operations that can be performed by the functional units are integer ALU, integer multiplication, floating point operations, load, store, Let assume the respective latencies be 1,2,3,2,1

Let the sequences of instructions as given below :

1. $y_1 = x_1 \times 10101$

2. $y_2 = x_2 \times 1001$

3. $z_1 = y_1 + 1011$

4. $z_2 = y_2 + 011$

5. $m_1 = m_1 + 1$

6. $q_1 = p_1 \times 101$

7. clr = clr +0010

8. r = r + 0010

Find out the minimum numbers of CPU cycles required to the complete execution of the instructions.

(c) Discuss and differentiate SIMD and MIMD architecture.

(d) Discuss the parallel algorithms design strategies.

SECTION – C

Note:- Attempt all questions. Attempt any two parts from each questions. $5 \times 8 = 40$

3. (a) Explain the different types of data dependency with a suitable example.

(b) Explain the Flynn's taxonomy of parallel computer model.

(c) Explain basic architecture of a distributed memory multiprocessor system.

4. (a) What do you understand by linear and non linear pipeline processor?

(b) What is the difference between scalar instruction and vector instruction?

(c) Explain associative and neural architecture also discuss recursive matrix multiplication algorithms with example.

5. (a) Differentiate between RISC and CISC processor architecture.

(b) Explain the terms memory bandwidth and fault tolerance.

(c) Explain the cache coherency in details.

6. (a) Write the advantages of cluster computing.

(b) Discuss the memory hierarchy in details.

(c) How to bridge the gap between the CPU and memory performance. Discuss the basic techniques for improving cache efficiency.

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